In the Claims:

Please amend claims 1-11, and add new claims 12-19 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) Method of manufacturing a semiconductor device ~~(10)~~ comprising a field effect transistor, in which method a semiconductor body ~~(1)~~ of silicon is provided at a surface thereof with a source region ~~(2)~~ and a drain region ~~(3)~~ of a first conductivity type, which regions are both provided with extensions ~~(2A,3A)~~, and with a channel region ~~(4)~~ of a second conductivity type, opposite to the first conductivity type, between the source region ~~(2)~~ and the drain region ~~(3)~~, and with a gate region ~~(5)~~ separated from the surface of the semiconductor body ~~(1)~~ by a gate dielectric ~~(6)~~ and situated above the channel region ~~(4)~~, and wherein a pn-junction between the extensions ~~(2A,3A)~~ and a neighboring part ~~(4A)~~ of the channel region ~~(4)~~ is formed by two implantations ~~(I_1, I_2)~~ of dopants of opposite conductivity type, and wherein before both of said two implantations ~~(I_1, I_2)~~ of dopants of opposite conductivity type are performed an amorphizing implantation ~~(I_0)~~ is performed where the pn-junction is to be formed, characterized in that the amorphizing implantation ~~(I_0)~~ and said two implantations ~~(I_1, I_2)~~ of dopants of opposite conductivity type are performed before the gate region ~~(5)~~ is formed and at an angle with the surface of the semiconductor body ~~(1)~~ which is substantially equal to 90 degrees.

2. (Currently Amended) Method according to claim 1, characterized in that a first implantation ~~(I_1)~~ of said two opposite conductivity type implantations ~~(I_1, I_2)~~ is carried out using a first mask ~~(M1)~~ covering a first region of the semiconductor body ~~(1)~~ and the second implantation ~~(I_2)~~ of the two implantations is carried out after removal of the first mask (M1), using a second mask ~~(M2)~~ of which the edge coincides with the edge of the first mask ~~(M1)~~.

3. (Currently Amended) Method according to claim 2, characterized in that the first mask ~~(M1)~~ and the second mask ~~(M2)~~ are formed in a self-aligned manner.

4. (Currently Amended) Method according to claim 2, characterized in that the first mask ~~(M1)~~ is formed by a dummy gate region ~~(5A)~~ of a first dielectric material, and the first implantation ~~(I_1)~~ is used to form the extensions ~~(2A,3A)~~ of the source and drain regions ~~(2,3)~~.

5. (Currently Amended) Method according to claim 4, characterized in that after the first implantation ~~(I_1)~~ a uniform masking layer ~~(40)~~ of a second dielectric material different from the first dielectric material is deposited on the semiconductor body ~~(1)~~ and is subsequently removed by chemical mechanical polishing from the top of the dummy gate region ~~(5A)~~ which is then removed by selective etching, the remainder of the masking layer ~~(40)~~ forming the second mask ~~(M2)~~ for the second implantation ~~(I_2)~~ which is used to dope the neighboring part ~~(4A)~~ of the channel region ~~(4)~~.

6. (Currently Amended) Method according to claim 5, characterized in that, after the second implantation ~~(I_2)~~, a uniform gate region layer ~~(50)~~ is formed on top of the semiconductor body ~~(1)~~ and is subsequently removed by chemical mechanical polishing from the top of the second mask ~~(M2)~~ which is then removed by selective etching.

7. (Currently Amended) Method as claimed in claim 1, characterized in that the ~~first and second~~ two implantations ~~(I_1, I_2)~~ are annealed at a temperature between 500 [[~~en~~]] and 700 degrees Celsius.

8. (Currently Amended) Method as claimed in claim 1, characterized in that the source[[-]] and drain regions ~~(2,3)~~ are formed before the source[[-]] and drain extensions ~~(2A,3A)~~.

9. (Currently Amended) Method as claimed in claim 1, characterized in that for the amorphizing implantation ~~(I_0)~~ ions are chosen from a group comprising Ge, Si, Ar or Xe.

10. (Currently Amended) Method as claimed in claim 1, characterized in that a part of the function of the amorphizing implantation ~~(I_0)~~ is provided by one of the two opposite

conductivity type implantations ~~(I_1, I_2)~~.

11. (Currently Amended) A semiconductor device ~~(10)~~ comprising a field effect transistor obtained with a method as claimed in claim 1.

12. (New) A method of manufacturing a semiconductor device comprising:

providing a semiconductor body having a surface;

forming source and drain regions of a first conductivity type at the surface of the semiconductor body;

performing an amorphizing implantation in a region of the semiconductor body where a pn-junction is to be formed;

performing a first implantation of dopants of the first conductivity type, in at least part of the region where the pn-junction is to be formed, to form source and drain extensions of the first conductivity type;

performing a second implantation of dopants of a second conductivity type opposite the first conductively type, in part of the region where the pn-junction is to be formed, to form a channel region of the second conductivity type, the channel region extending between the source and drain extensions, thereby forming the pn junction;

forming a gate dielectric on the surface of the semiconductor body above the channel region; and

forming a gate region on the gate dielectric,

wherein the amorphizing implantation is performed before the first and second implantations, and wherein the amorphizing implantation and the first and second implantations are performed before the gate region is formed and at an angle with the surface of the semiconductor body that is substantially equal to 90 degrees.

13. (New) The Method according to claim 12, further comprising forming a first mask on a first region of the semiconductor body where the channel region is to be formed prior to performing the first implantation; forming a second mask on the semiconductor body after performing the first implantation, edges of the first mask coinciding with

edges of the second mask; and removing the first mask prior to performing the second implantation, the second implantation being carried out using the second mask.

14. (New) The Method according to claim 13, wherein the first mask and the second mask are formed in a self-aligned manner.

15. (New) The Method according to claim 13, wherein the first mask is formed by a dummy gate region of a first dielectric material.

16. (New) The Method according to claim 15, wherein the second mask is formed by depositing a masking layer of a second dielectric material, different from the first dielectric material, on the semiconductor body and subsequently removing, by chemical mechanical polishing, the second dielectric material from the top of the dummy gate region, the dummy gate region then being removed by selective etching prior to performing the second implantation.

17. (New) The Method according to claim 16, wherein the gate region is formed by depositing a gate region layer on top of the semiconductor body after performing the second implantation and subsequently removing, by chemical mechanical polishing, the gate region layer from the top of the second mask, the second mask then being removed by selective etching.

18. (New) The Method according to claim 12, further comprising annealing the first and second implantations at a temperature between 500 and 700 degrees Celsius.

19. (New) The Method according to claim 12, wherein the source and drain regions are formed before the source and drain extensions.